

# High-Density 3D: Progress and Problems

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TSVs, wafer bonding, 3D interconnects, TLP bonding, 3D standards for “via-out” locations

Several proprietary processes exist for manufacturing high-density 3D TSV-based commercial products

Higher density 3D with direct die-to-die interconnection has been a major industry goal for the past decade. As transistors shrink toward affordable lithographic pattern horizontal scaling limits, growing vertically becomes an attractive alternative. Direct local die-to-die vertical interconnection of internal circuit functions with heterogeneous integration is the final goal. Local 3D interconnection of die to die will shorten signal paths, increase speed and packing density, and reduce power consumption and cost.

## Status

Wire bonded stacks of 4 to 8 memory die have been commercially available for years. Interconnections are between standard input and output pads, which are now referred to as global interconnects, rather than local interconnects from within the die. These indirect signal paths slow transmission and waste power. Often the wires become the greatest source of power dissipation and may become RF antennas with associated problems. High-density through-silicon vias (TSVs) connecting vertically from die-to-die are the leading solution.

Basic TSVs are well proven, with commercial applications in CMOS imagers and MEMS arrays. Silicon interposers are a possible near-term alternative. Pieces of silicon with TSV connect die and circuitry mounted on the upper and lower sides. The interposer approach – sometimes referred to as 2.5D integration – is completing qualification. Interposers may be adopted as interim solutions until finer pitch TSVs for direct local interconnection from die to die within a stack are commercially available.

Currently, more than 50 companies are involved in commercializing high density 3D. Fifteen different 300 mm 3D-IC pilot production lines are reported to be currently being installed or in operation. Yole Développement forecasts (Figure 1) that the market for 3D integration using TSVs will grow from slightly less than \$500 million in 2010 to over \$4 billion in 2015, a compounded annual growth rate of 52%.<sup>1</sup>

CMOS sensor applications continue to grow. More complex applications are expected to phase in over the next several years, with “logic + memory” system-in-package modules finally becoming dominant at about 40% of the 2015 total market.

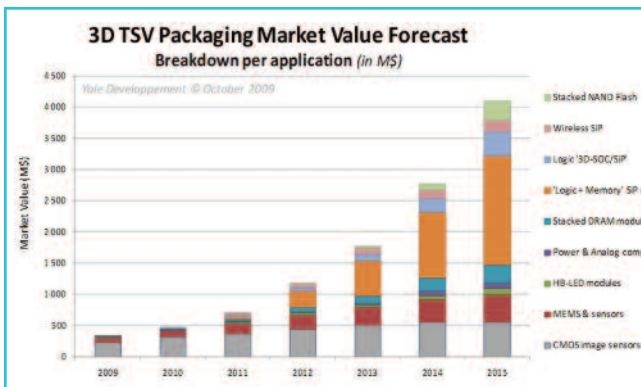


Figure 1. TSV Market Forecast. (Courtesy Yole Développement).

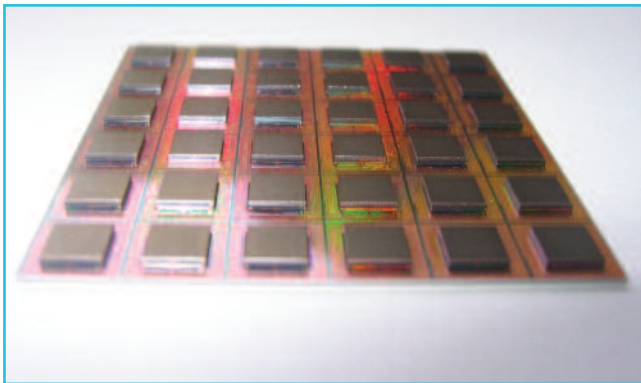


Figure 2. TLP bonding of stacked die. (Courtesy IMEC).

## Progress

As fine pitch TSVs move toward pilot production, the current technical challenge is how to best handle, stack and bond thinned TSV die and wafers. A collection of leading-edge technical papers from SET S.A.S reveals the wide variety of 3D approaches that different companies are developing.<sup>2</sup>

For example, CEA/Leti-MINATEC is implementing direct die-to-wafer bonding without polymer layers, to produce a thinner die stack with reduced thermal strain and wider post-processing limits.<sup>3</sup> A low-stress oxide inter-die filling provides planarization. In contrast, IMEC uses a tacky polymer as an intermediate glue layer. This layer can hold many precisely placed die for simultaneous bonding, optimizing throughput by separating pick-and-place from the bonding operation.<sup>4</sup>

IMEC has also developed a sequential die stacking process for adding more die without disturbing the lower stack. Transient liquid phase (TLP) bonding creates a higher melting point bond after soldering, so that subsequent die may be soldered in the stack without disturbing earlier layers (Figure 2).<sup>5</sup>

RTI International has compared thermocompression bonding of copper-to-copper (Cu-Cu) bumps with solid-liquid diffusion bonding between Cu and copper/tin (Cu/Sn) bumps (Figure 3). They find that Cu/CuSn bonding will better compensate for surface irregularities, but Cu/Cu bonding yields stronger bonds than Cu/CuSn. Stronger bonds more readily allow mixing die with differing thermal expansion coefficients in heterogeneous stacks.<sup>6</sup>

Most developers prefer to fill high aspect ratio TSVs from the top side down, but ITRI reports cost and throughput advantages

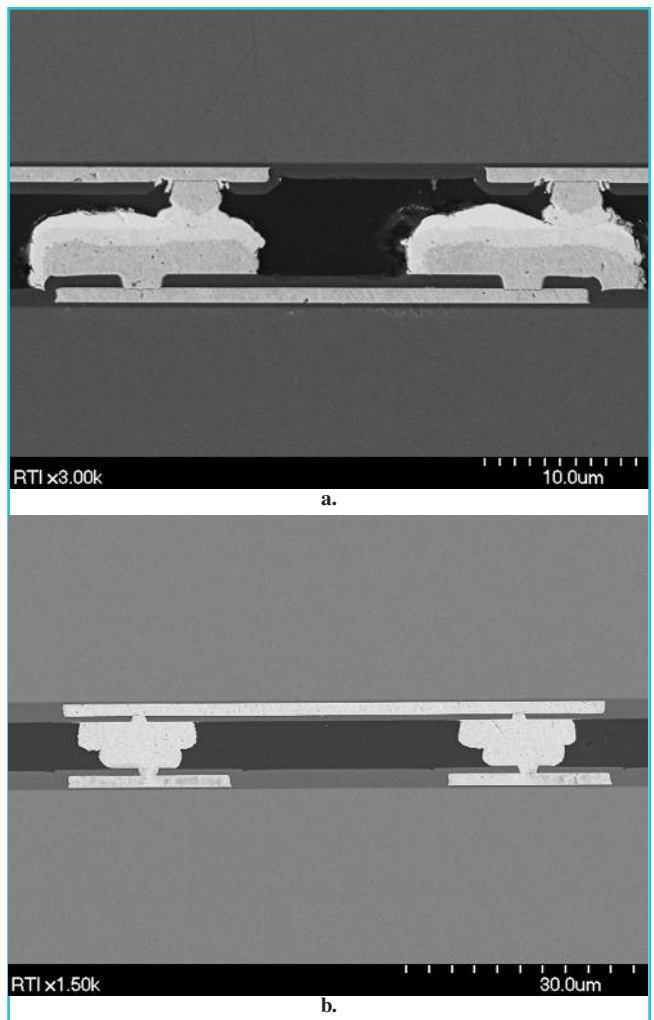


Figure 3. a) Cu/ CuSn bonding. (Courtesy RTI International). b) Cu/Cu bonding. (Courtesy RTI International).

of bottom-up filling (Figure 4).<sup>7</sup> Advantages include eliminating the expensive MOCVD deposition of a seed layer, and using DC copper plating with a standard bottom-up plating machine and ordinary plating solutions.

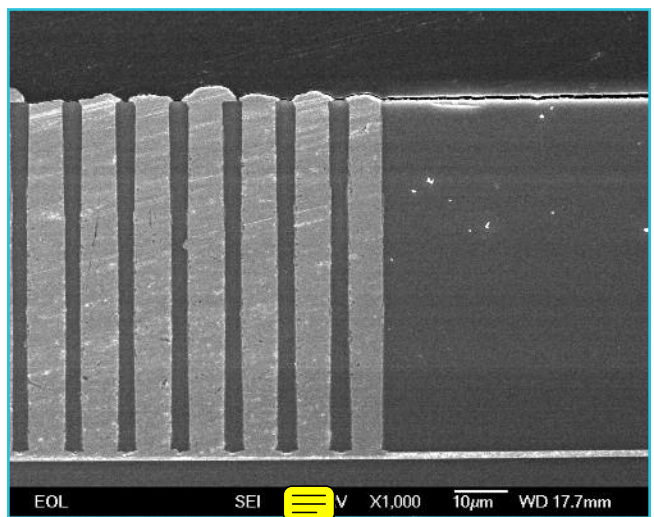


Figure 4. Bottoms-up TSVs, 5µ pitch solder bumps. (Courtesy ITRI).

Bottom-up plating is independent of the DRIE angle and is unaffected by sidewall scallops. Bottom-up plating shortens TSV fabrication time to 1.5 hours from the usual 3 to 12 hours, producing void-free vias with higher throughput and lower cost.

IME-A\*STAR reports advantages of 2  $\mu\text{m}$  thick electroless nickel-immersion gold (ENIG) as UBM for 15  $\mu\text{m}$  pitch plated Cu/Sn solder microbumps (Figure 5).<sup>8</sup> Nickel barrier structures give Cu/Sn bumps electromigration lifetimes equal to or better than lead/tin (Pb/Sn). For these very fine pitches, common UBMs are difficult to pattern with photolithographic patterning and wet etching because of undercutting of the pads. Nickel provides an effective pad without requiring either photopatterning or etching.

One area of convergence in 3D appears to be a shift toward die-to-wafer bonding for most complex applications. Wafer-to-wafer (W2W) bonding was common in much early 3D work. W2W provides faster throughput, because it simultaneously bonds all of the devices onto the wafer.

Bonding die to a wafer one-by-one takes more time. However, recent advances in die-to-wafer (D2W) bonding now allow all die to be placed or even stacked onto the wafer before simultaneously bonding all of them (Figure 6).

D2W assembly has many advantages over W2W. Separately mounting only tested die onto the wafer allows matching them only to known good wafer die, raising final yields. Single die are quickly aligned and placed over typical distances of a few millimeters. W2W alignments over much longer distances are slower and risk yield loss from wafer flatness deviations and from thermal expansion differences.

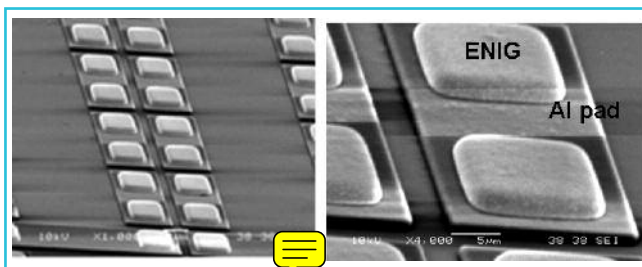


Figure 5. ENIG pads for 15  $\mu\text{m}$  pitch solder bumps. (Courtesy IME-A\*STAR)

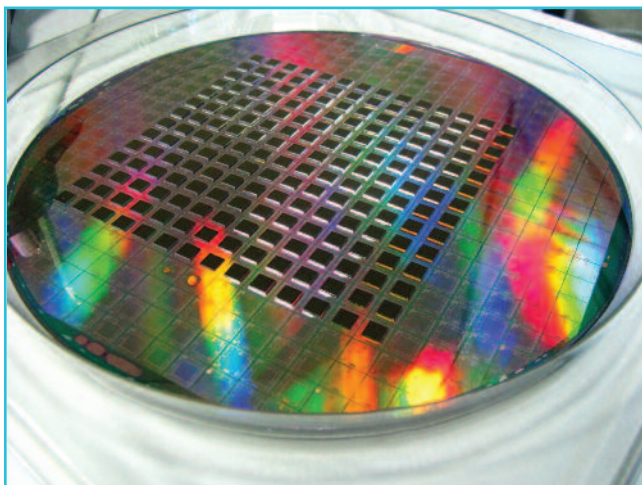


Figure 6. Die sequentially placed, simultaneously bonded. (Courtesy IMEC)

D2W assembly readily accommodates heterogeneous mixes of die, including unequal die sizes and thicknesses within a stack; W2W does not.

A key enabler of 3D development is timely availability of advanced equipment. Advanced bonders for 3D must accommodate the wide range of process parameters demanded by competing companies trying to establish their own proprietary process flows.

For example, bonding may be D2D or D2W. Many different solder alloys and processes are in use. Thinned die and wafers require careful handling. Post-bond placement accuracy below 1  $\mu\text{m}$  is advantageous. Automatic leveling of die to the wafer, or even self-leveling, is desirable.

Close control of temperature profiles and of the bonding force profile, duration and pressure is essential to assure the required bond strength and to meet the long-term reliability goals. Automatic line monitoring and process controls are required for higher line throughputs and lower costs.

### Problems

3D/TSV technical problems now being addressed include developing common design tools, implementing standards, establishing supply chains, handling thermal hot spots, and demonstrating long-term reliability. Simply adding 3D elements to today's 2D designs will not maximize the benefits of 3D. Taking advantage of features such as direct local die-to-die connection and repartitioning requires a system redesign with new tools.

Heterogeneous die stacking will require integrating die from different manufacturers. Standards are needed to ensure common interfaces among die from different suppliers. Just as JEDEC standards today specify pin-out locations, 3D standards will be needed tomorrow to specify "via-out" locations. JEDEC's first 3D/TSV reliability methodologies standard appeared in November 2009.

A major supply chain question is where in the production line will TSVs be created: early in wafer fabrication, at a later stage in wafer processing ("middle-of-line"), or at the end, as part of packaging? The answer affects both via processes and via locations. It also determines who in the supply chain does the job, wafer suppliers or packaging houses. Much current opinion favors middle-of-line over front-end or back-end approaches.

Thermal control raises performance and reliability issues. While die stacks have many advantages, heat dissipation is not one of them. In today's 2D layouts, a die can use an exposed back side for cooling or heat sinking. Within a stack, neither side of a die may be available, and local hot spots could occur. Liquid cooling, carbon nanotube heat sinks, and thermal vias are among the possible thermal options.

Industry TSV reliability questions highlight the differing TSV approaches being pursued. For instance, in late 2008, Tezaron Semiconductor announced it was switching from copper-filled TSVs to tungsten-filled. The reason was to eliminate reliability problems that they discovered from the disruptive thermal expansion of copper, a condition now known as "copper pumping."

IMEC later stated that copper filling of TSVs is reliable if the copper is properly annealed after deposition. A still later IBM reliability report showed that both copper and tungsten annular

fillings are reliable if properly designed and deposited, but that tungsten filling gives higher reliability than copper.

## Conclusions

Industrialization of high density TSVs continues to progress. Technical problems remaining to be solved include design, standards, supply chain, thermal and reliability areas. Design systems and standardization will appear when commercial needs are clearly established.

Some of the many development processes may converge, but both the diversity of goals and the competitive drive for proprietary processes make a single, “one-size-fits-all” process unlikely. Equipment suppliers currently assisting commercialization will develop more specialized equipment as the needs become clear.

Cooperative efforts of equipment suppliers and research/development teams should carry die-to-die interconnection of complex functions with TSV-based 3D phasing into high-volume production over the next five years.

## References

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